

mm-Wave Imaging Radar

DESIGN DOCUMENT

Team 20

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Team Members/Roles:

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Nathan Ayers - User Interface

Rodrigo Romero - SPI Implementation (FPGA)

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Executive Summary

Development Standards & Practices Used

- IEEE 287.1-2021, IEEE 287.2-2021, IEEE 287.3-2021 (Pertains to Precision Connectors at RF, Microwave, and Millimeter-Wave Frequencies.)
- IEEE 1696-2013 (Terminology and Test Methods for Circuit Probes.)
- IEEE 1658-2011, IEEE 1241-2010 (Terminology and Test Methods of Digital-to-Analog Converter Devices, and Analog-to-Digital.)

Summary of Requirements

- Digitally generate a sinusoidal signal with a frequency of 5 to 60 MHz.
- Output Signals through a DAC to the mm-wave radar.
- Return the output of the mm-wave radar (5 to 60 MHz) using an ADC.
- Use an FPGA to generate the sinusoid (SPI) and sample the output signal (DSP)
- The FPGA will send the data to a PC using USB.
- Program an application on the PC to interface with the FPGA.
- Design PCB for the FPGA to interface with the ADC and the DAC, respectively.

Applicable Courses from Iowa State University Curriculum

- EE 285: Learned how to write simple but useful algorithms in C. This will be somewhat helpful for writing PC interface code, especially for organizing the processed data from the FPGA into a file.
- CPRE 288: Learned how to interface with microcontrollers and their corresponding GPIO pins, which will be useful for the USB communication with our FTDI chip, and programming its GPIO pins, etc.
- CPRE 281: Learned how to write in Verilog at a very basic level, we may program the FPGA in Verilog or use a processor to convert C code into Verilog/VHDL.
- EE 311/411: Provided background knowledge on the purpose and use of mm-wave radar.

New Skills/Knowledge acquired that was not taught in courses

- Programming in Windows, this is Nathan's first time programming outside of a Linux environment, where things are usually contained a little differently. He also has no experience installing specific drivers for communicating over USB. Specifically, the drivers are from FTDI (Future Technology Devices International Limited) they create the chips that are being used for PC communication with the FPGA. They are open source, and for this project, he is using the D2XX and D3XX drivers.
- Rodrigo and Michael have limited FPGA experience, so this will be their first experience with Vivado, which is the recommended Software for synthesizing and analyzing HDL. They will have to acquire new skills to use the software, but we can assume that there will be high-quality documentation given by the manufacturer, Xilinx.
- Matt is well acquainted with PCB design from his work background, the main challenge will be to understand the pin placement of the alchitry boards provided, given the minimal detail provided on the datasheets.

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1 Team

1.1 TEAM MEMBERS

Nathan Ayers (Electrical Engineering), Matthew Caron (Electrical Engineering), Michael Levin (Electrical Engineering), Rodrigo Romero (Electrical Engineering).

1.2 REQUIRED SKILL SETS FOR YOUR PROJECT

- PCB design & Hardware Integration: Necessary to integrate the FPGA, ADC, and DAC.
- Soldering: Will be needed for device integration and testing. But most importantly, we must mimic the header connections on the boards we produce so they match what we already have, requiring soldering.
- FPGA programming: Needed to create the output signal to the mm-wave radar and for sampling the returned signal from the radar. Also needed to interface with the PC.
- Digital Signal Processing: The input signal sampling described in the requirements refers to the decomposition of the signal into its real and imaginary components, which the FPGA will do.
- PC communication with FPGA via FTDI chip: Necessary to connect the PC to the FPGA, which connects the user. The PC will initiate the generation of the output signal by the FPGA by communicating with the FPGA and will also read the processed signal from the Signal Processing block and then store that for the user.
- UI (GUI): The requirements asked for an application to communicate with the FPGA. This takes some of the burdens off of the user and, if done correctly, should make for a faster process every time.

1.3 SKILL SETS COVERED BY THE TEAM

- Nathan Ayers: PC communication with FPGA via FTDI chip, UI (GUI), FPGA programming
- Matthew Caron: PCB design & Hardware Integration, Soldering, FPGA programming
- Michael Levin: FPGA Programming, Digital Signal Processing
- Rodrigo Romero: FPGA Programming

1.4 PROJECT MANAGEMENT STYLE ADOPTED BY THE TEAM

Following a Waterfall Workflow, as our project has built on itself, meaning that assignments or roles for some of us are dependent on others finishing their roles. It may look like an Agile system, but we are not doing any Agile methodologies. We are essentially preparing for our turn to integrate our work into the project, and in the meantime, we know what we need to be building toward and will practice and run simulations with sample or fake data.

1.5 INITIAL PROJECT MANAGEMENT ROLES

- Nathan Ayers: Interface Lead
- Rodrigo Romero: Lead FPGA Programming Engineer
- Matthew Caron: Lead Hardware Designer
- Michael Levin: Lead DSP Engineer

2 Introduction

2.1 PROBLEM STATEMENT

Over the last few decades, the prominence of mm waves in nondestructive evaluation has been recognized for its important features. The Iowa State Center for Nondestructive Evaluation lists features that include the ability to penetrate dielectric (non-conducting) materials, high sensitivity to small material flaws due to small wavelengths and large available signal bandwidth, and the technology is easy to use. And given recent breakthroughs in mm-wave technology, such as the noninvasive diagnosis of human skin for cancer, this has future implications. Therefore, this is the perfect tool to put in a student or researcher's hands here at Iowa State. Not only will they be able to use it for research purposes, but they can also be on the leading edge of mm-wave technology and create something better. Our goal is to put a mm-wave imaging radar in the hands of those students.

2.2 REQUIREMENTS & CONSTRAINTS

Functional requirements (specification)

- Must interface with inherited hardware/software that includes an Up counter and Down counter; this will require us to deliver an output signal to the Up counter via a DAC and to return an input from a down counter through an ADC. (constraint).
- Our design will ideally output a 10 MHz signal, which will be “sped up” by the existing hardware (Up counter). We are constrained by the clock speed of our FPGA
- With the input signal returned from the mm-wave radar, we must convert that into its real and imaginary components.
- Communicating with PC to FPGA via a USB-C port.
- Any PCB designs that interact with the FPGA and its connected pins must connect to the four sections of surface mount headers with .1” spacing (constraint).

Qualitative aesthetics requirements

- While not discussed in depth with the client, the understanding is that this design must be packaged, and it contains at least five PCBs, with some conveniently mounting onto each other; we will also have openings for USB ports. The current aesthetic for packaging seems to be either 3D printing or sheet metal.

Economic/market requirements

- Our design doesn't have any market requirements as it will be used for research experiments by students at the CNDE, but we are constrained by the amount of funding that our project has. Much of our funding has been used for our FPGA and, eventually, our ADC and DAC (constraint).

UI requirements

- Must have a GUI, the PC code should be invisible to the user, so this limits the possible programming languages to C#, Python, and others. Other language constraints will be determined by the programmer (constraint).
- This converted data must be organized clearly into a file on the PC so that Labview or Matlab may graph it.

2.3 ENGINEERING STANDARDS

IEEE 287.1-2021, IEEE 287.2-2021, IEEE 287.3-2021:

These three standards relate to Precision Connectors at RF, Microwave, and Millimeter-Wave Frequencies.

- We require connectors capable of transmitting and receiving the required data and wave functions at the given frequencies. This will mostly consist of megaHertz transmission for data going in and out of the antenna and GigaHertz transmission that will be transmitted from the antenna itself. Between the devices, this discrepancy in data speed means that very particular connectors are needed. The PDF goes into great detail on a variety of different-sized connectors, which will be important to us when making decisions about purchasing connectors, as we will want to know about the ideal characteristics of the connectors.

IEEE 1696-2013:

IEEE Standard for Terminology and Test Methods for Circuit Probes.

- Our project requires an input and output to be connected to existing hardware previously designed by ISU researchers. So much like the standards discussed above, we need to be knowledgeable about connection standards, as the design will transmit high-frequency signals. The article for this standard focuses primarily on Oscilloscopes, the first use of a probe that would come to mind for most Electrical Engineers. It does mention VNAs, which we are building as part of our project, we are sending a sinusoidal wave and will receive a sinusoidal output. The article mentions how to calibrate the probes and measure important parameters, we will probably not have the luxury of time to obtain different probes and measure the parameters, but we can search for probes with desirable parameters and features now that we know which are important, such as input/output resistance, gain, error, and step response.

IEEE 1658-2011, IEEE 1241-2010:

IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices, and Analog-to-Digital.

- Our project hinges on the DAC and ADC functioning properly. They are the junctions of the data flow between the FPGA and the antenna and will be paramount in the reception and transmission of high-speed data. This means that they will require an abundance of

testing. This must be thorough and multifaceted because of how many physical and digital components go into these devices' functions.

2.4 INTENDED USERS AND USES

This design and the final product have very niche uses, which is normal for advanced instruments such as DAQs (Data Acquisition). In the project abstract, Dr. Tayeeb states that this system will be used to conduct radar imaging experiments in the microwave lab at the CNDE (Center for Nondestructive Evaluation). This project will never see the outside of Iowa State, but similar projects are likely happening worldwide; mm-Wave imaging radar can be used for range measurements, velocity measurements, and even for detecting angles [1]. Our design will end up in the hands of future students and student researchers here at Iowa State, and they will have a background or focus in either electromagnetics or communications and signal processing.

3 Project Plan

3.1 PROJECT MANAGEMENT/TRACKING PROCEDURES

Most of the work for the development of the intermediate frequency circuit requires coding, to keep updating it, the team is using the Iowa State University platform "GitLab". Besides that, the team will be keeping track of the tasks using a Gantt chart. Base on the Gantt chart, it can be inferred that the project management style adopted for the team is a mix of agile and waterfall.

This will work this way because to reach the integration of the system some subsystems, and tasks need to be accomplished by different team members, some of them at the same time, some others activities will be dependant on a team member finishing their tasks before continuing the project.

3.2 TASK DECOMPOSITION

In order to solve the problem at hand, it helps to decompose it into multiple tasks and subtasks and to understand interdependence among tasks. This step might be useful even if you adopt agile methodology. If you are agile, you can also provide a linear progression of completed requirements aligned with your sprints for the entire project.

Here are explained the tasks involved in building the intermediate frequency (IF) circuit for a mm-wave imaging radar.

Frequency conversion: The incoming millimeter wave signal will be down-converted to an IF in the range of gigahertz. This frequency conversion will be performed by a mixer that combines the incoming signal with an FPGA.

Amplification: The down-converted signal is will be amplified by one or more stages of RF amplification to increase the signal strength and improve the signal-to-noise ratio.

Filtering: The amplified signal will be filtered to remove any unwanted noise or interference. This will be done using digital signal processing filters that only allows signals in the desired frequency range to pass through.

Demodulation: In this radar system, the down-converted signal will be further demodulated to extract the phase and amplitude information of the received signal.

Analog-to-digital conversion: The filtered and demodulated signal will be converted from an analog signal to a digital signal using an analog-to-digital converter (ADC). This will allow the signal to be processed by the radar's digital signal processing system. For the further development of the project, there will be needed extra activities that describe specific details about the project such as: design of FPGA to DAC/ADC, manufacture of the board, development of hardware attachments, development of code to perform data acquisition, code to perform data communication.

Once the project is completed the tasks will continue to be in testing aspect.

Testing in communication system.

Testing of signal generation.

Testing of data acquisition system.

Testing of the integrated system.

3.3 PROJECT PROPOSED MILESTONES, METRICS, AND EVALUATION CRITERIA

The project-proposed milestones, metrics and evaluation criteria is defined as follows.

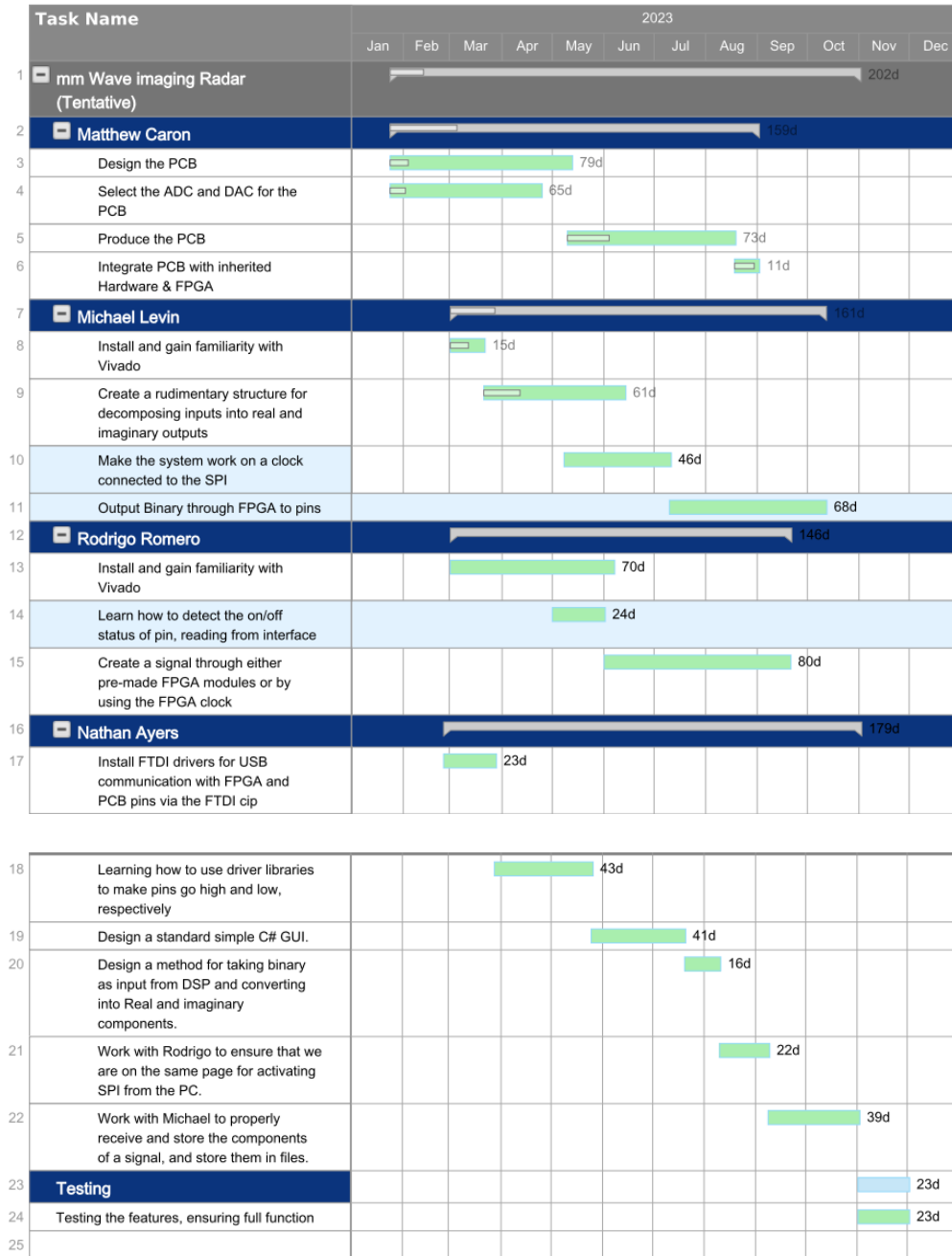
Schedule adherence: This will measure whether the project is on track to meet its deadlines and milestones. It will be measured by tracking the progress of individual tasks and comparing them to the project schedule.

Client satisfaction: This measures the satisfaction of project stakeholder, including the project sponsor, and end-users. This aspect will be measured by conducting conversations and meetings with the project client, and gathering feedback on the project's progress and deliverables.

Team performance: This will measure the performance of the project team. It can will measured by tracking team member productivity, collaboration, and communication.

3.4 PROJECT TIMELINE/SCHEDULE

Project Launch Plan



- We plan to have the hardware finished by the end of Summer to give us a good foundation to finish the programming parts in the next semester
- By the end of September, we expect to have the SPI done.
- We expect to finish the interface and correct any bugs by the end of November
- We will use our remaining time to polish the device and test it thoroughly

3.5 RISKS AND RISK MANAGEMENT/MITIGATION

Design of FPGA to DAC/ADC. Risks associated with milestones reached can be expected due to inconveniences during the project execution.

Manufacture of the board. A risk associated with the manufacturing process of the board could be the time delay due to supply chain issues.

Development of hardware attachments. Once the project is at a 75% of development it will be necessary to create parts to group all the components and subsystems of the radar. With this, time issues can come in the sense of creating the parts since we rely on 3D printing parts to achieve this task. The 3D printer available may not function properly so it will represent a time delay.

Development of code to perform data acquisition. In this stage of the project, the associated risk is that the code developed would not function as expected. This is a sensitive point for the team since no one is specialized in software or computer engineering. The way will mitigate this risk is having help from a member of the Center for Non-Destructive Evaluation whom part of their expertise is software development.

3.6 PERSONNEL EFFORT REQUIREMENTS

Include a detailed estimate in the form of a table accompanied by a textual reference and explanation. This estimate shall be done on a task-by-task basis and should be the projected effort in total number of person-hours required to perform the task.

Name	Job	Time(est.)
Matt	Design the PCB, produce the PCB	40 hours
Matt	integrate with pre-existing hardware components.	20 hours
Matt	Source ADC & DAC	15 hours
Rodrigo	Alquistry Lab manipulation at a high level	30 hours
Rodrigo	Verilog code for communication between radar and PC	25 hours
Rodrigo	establish the frequency regulation program	25 hours

Michael	Create a rudimentary structure for decomposing inputs into real and imaginary outputs	15 hours
Michael	make the system work on a clock connected to the SPI	15 hours
Michael	make the input and output into binary signals	10 hours
Michael	Optimize DSP	20 hours
Nathan	Communicate w/ FTDI chip	25 hours
Nathan	Write to FPGA pins	20 hours
Nathan	Read from FPGA pins	20 hours
Nathan	Program to save data into a usable file.	25 hours

4 Design

4.1 DESIGN CONTEXT

4.1.1 Broader Context

Millimeter wave (mm-wave) radar has shown great potential in non-destructive evaluation (NDE) applications due to its ability to penetrate dielectric materials and detect hidden defects. Some examples of how mm-wave radar can be used in NDE are: detection of cracks and corrosion, evaluation of concrete structures, inspection of composites, measurement of thickness.

This design is intended to be used by researchers students and lab technicians at the Center for Non-Destructive Evaluation at Iowa State University. Once finished and evaluated, this project can be a great potential to substitute equipment that usually entails large prices.

List relevant considerations related to your project in each of the following areas:

Area	Description	Examples
Public health, safety, and welfare	Due to its contactless nature, a millimeter-wave radar has potential applications in public health such as non-invasive health monitoring, disease detection, and mobility aids. However, further research is needed to fully explore this area.	Can be used to detect abnormalities in tissue that may be indicative of disease, such as tumors or other irregularities. It also can be used to help people with disabilities to move around more independently.
Global, cultural, and social	How well does your project reflect the values, practices, and aims of the cultural groups it affects? Groups may include but are not limited to specific communities, nations, professions, workplaces, and ethnic cultures.	Development or operation of the solution would violate a profession's code of ethics, implementation of the solution would require an undesired change in community practices
Environmental	By utilizing a non destructive method in understanding, components, and being able to see what is inside of a structure, it is avoided the necessity of destructing a piece of equipment to see what is inside of it.	Mm-wave radar can be used to evaluate the quality of concrete in buildings, bridges, and other structures. The radar can detect voids, delamination, and other defects that may affect the strength and durability of the structure.
Economic	Developing an efficient, precise, and cost effective millimeter-wave radar, an entity can become competitive in addressing the obstacle of economic due to the high price of such equipment.	One of the uses of a millimeter-wave radar is to measure dielectric thicknesses. A lab can substitute a Vector Network Analyzer to do this measurements.

4.1.2 User Needs

A research student needs a millimeter-wave radar to study the imperfections of different materials because there is a great potential for applications in the NDE field.

A lab technician needs a mm-wave radar to examine the infrastructure of an old concrete building because it has been diagnosed as “risk to live in”.

4.1.3 Prior Work/Solutions

Claire M. Watts, Patrick Lancaster, Andreas Pedross-Engel, Joshua R. Smith, and Matthew S. Reynolds. 2D and 3D Millimeter-Wave Synthetic Aperture Radar Imaging on a PR2 Platform. 2016 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) Daejeon Convention Center October 9-14, 2016, Daejeon, Korea.

Xiaoxuan Zhang, Jie Liang, Nan Wang, Tianying Chang , Qijia Guo, and Hong-Liang Cui. Broadband Millimeter-Wave Imaging Radar-Based 3-D Holographic Reconstruction for Nondestructive Testing. IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 68, NO. 3, MARCH 2020.

This project is not following previous work developed, it is to show alternate ways to develop some of the NDE required tasks. However, there are some works that this project will utilize as a reference of the uses and applications for the NDE field.

4.1.4 Technical Complexity

The digital signal processing requires mathematical complexity such as inverse fast Fourier transforms to move from the frequency domain to the time domain.

This project involves a lot of coding and low level programming to develop the communication system between the FPGA and the PC.

Imaging radar requires understanding of wave of physics to be able to design and develop a reliable source of signal.

4.2 DESIGN EXPLORATION

4.2.1 Design Decisions

To create enclosure of the circuit and some of the pieces our design will be using, we decided to use PLA material because of its lightweight and its nonconductive nature.

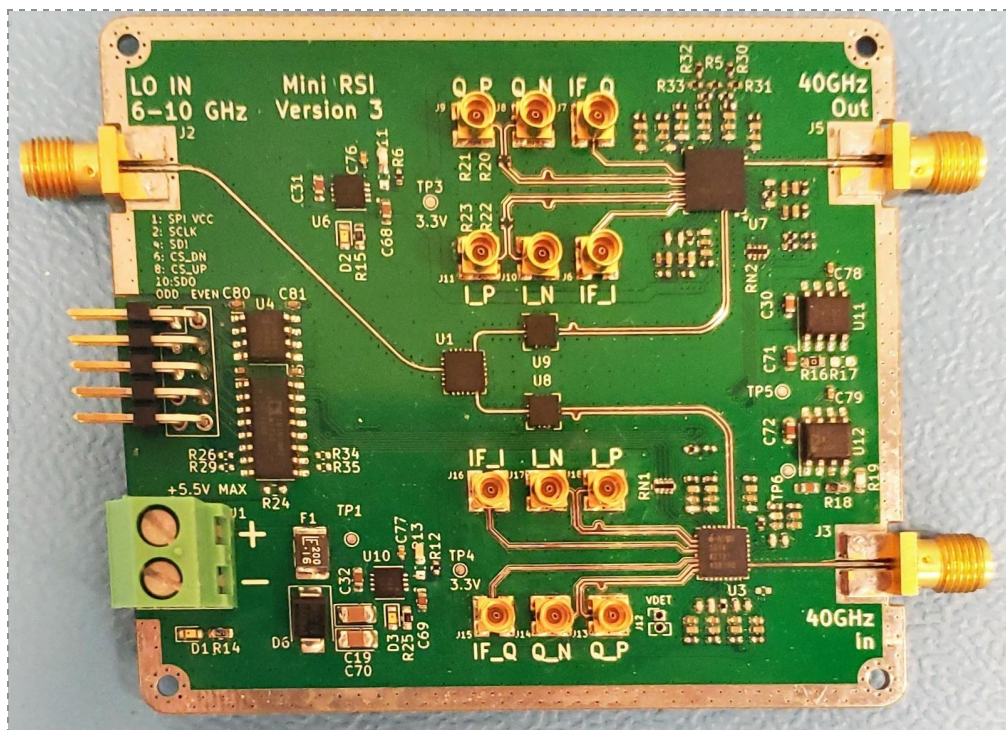
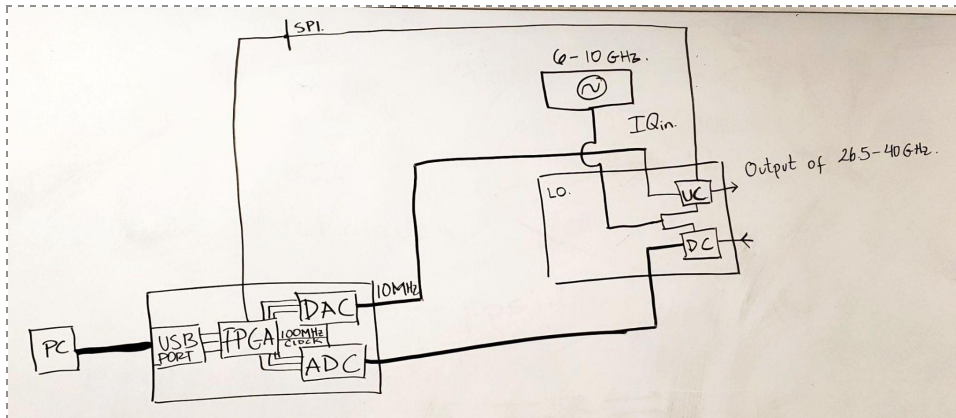
4.2.2 Ideation

For the material enclosure of the circuit we discussed about metal, wood, and plastic materials. For durability, feasibility, and adjustability to design we decided to work with PLA.

4.3 PROPOSED DESIGN

At this point, what we have started to experiment is with the communication between a PC and the future USB connection that will be established with the FGPA.

4.3.1 Design Visual and Description



4.3.2 Functionality

The deliverable is intended to be properly working in a lab environment, used as a tool to make measurements to evaluate a certain material, part, or sample.

4.3.3 Areas of Concern and Development

The concern is more about software. Coding and programming is a skill none of us have it mastered.

5 Testing

5.1 UNIT TESTING

Units that will be tested include the FPGA design which include the following: SPI outputs (making sure we are writing the correct data to the correct registers in each of the chips, the digital inputs to the DACs (making sure the correct signal is being output), and the ULPI data input and output data is correct for USB communication. The other unit that should be tested is the PCB which includes the following: making sure the ADC and DAC filters have the correct cutoff frequencies and checking to make sure that the DACs are outputting the correct signal and the ADCs are receiving the correct signals.

5.2 INTERFACE TESTING

The interfaces include: the PCB/FPGA and the APP for imaging. To test the PCB and FPGA we will give it a known sample and ensure the signal processing is manipulating and outputting the signal correctly. Finally to test the APP we will send known data through USB then make sure its plotting the correct data.

5.3 INTEGRATION TESTING

The integration testing will consist of separate subsystems integration. The first one will be between the PC and the FPGA.

On the other hand, the integration testing will be executed to ensure the communication between the FPGA and the different components that it will be communicating with.

5.4 SYSTEM TESTING

After testing individual components and ensuring they are robust we will then use the device as intended until we are sure it is performing properly. To do this we will connect the device to a matched antenna and test the device for imaging previously measured materials and compare the results.

5.5 REGRESSION TESTING

To ensure that new additions don't break our device we have implemented a number of structural safeguards. Most obvious of these is our waterfall structure which prevents any new component from being added before all of the previous products work together well. We will also have thorough testing of all of the individual components and have prioritized the functionality of each component in order of where they fall in the waterfall structure (hardware, SPI, DSP, and the interface).

5.6 ACCEPTANCE TESTING

To ensure that new additions don't break our device we have implemented a number of structural safeguards. Most obvious of these is our waterfall structure which prevents any new component from being added before all of the previous products work together well. We will also have thorough testing of all of the individual components and have prioritized the functionality of each

component in order of where they fall in the waterfall structure (hardware, SPI, DSP, and the interface).

5.7 RESULTS

Even though we have not completed testing yet we can look at what our device should be capable of...

- Confirming the FPGA is programming the correct SPI registers
- Analysis to confirm we are outputting and receiving the correct signals (DACs, ADCs, USB phy, ect.)
- Measuring a known material and comparing results to what we expect

6 Implementation

Once the PCB has been manufactured and assembled we need to start implementation of hardware on the FPGA. This will include implementing SPI ports on the FPGA that correspond to lines on the PCB. After which we need to implement DSP (digital signal processing) on the FPGA for processing input signals from the ADCs

7 Professionalism

This discussion is with respect to the paper titled “Contextualizing Professionalism in Capstone Projects Using the IDEALS Professional Responsibility Assessment”, *International Journal of Engineering Education* Vol. 28, No. 2, pp. 416–424, 2012

7.1 AREAS OF RESPONSIBILITY

Pick one of IEEE, ACM, or SE code of ethics. Add a column to Table 1 from the paper corresponding to the society-specific code of ethics selected above. State how it addresses each of the areas of seven professional responsibilities in the table. Briefly describe each entry added to the table in your own words. How does the IEEE, ACM, or SE code of ethics differ from the NSPE version for each area?

Area of responsibility	Definition	Brief description	Difference from the NSPE version
Work Competence	Perform work of high quality, integrity, timeliness, and professional competence.	Explains the quality of the work expectations that will be delivered from an engineer.	NSPE talks about the engineer capabilities depending on their specialization.
Financial Responsibility	Deliver products and services of realizable value and at reasonable costs	Offers viability in their solutions. The engineer solve a necessity or a problem	NSPE does not mention explicitly the financial responsibility to the

		considering the economic factor.	population economy.
Communication Honesty	Report work truthfully, without deception, and understandable to stakeholders.	Express themselves clearly and in an understandable, honest, and transparent way to their audience.	NSPE includes the limitation that engineers should have about not speaking in favor of determined interests.
Health, Safety, Well-Being	Minimize risks to safety, health, and well-being of stakeholders.	In their projects, engineers, consider the safety of the users by minimizing risks in their designs.	NSPE does not talk about safety instead mentions all limitations an engineer has to protect private information.
Property Ownership	Respect property, ideas, and information of clients and others.	Engineers are expected to give proper credit to others' ideas.	NSPE limits the engineer to disclose private information.
Sustainability	Protect environment and natural resources locally and globally.	Engineers are ecologically responsible by taking care of the potential risks associated to damages over the Earth.	NSPE does not explicitly talk about the care should be taken by engineers with the environment.
Social Responsibility	Produce products and services that benefit society and communities.	Engineers are expected to have social consciousness by solving problems for the majority of the population.	NSPE includes that engineers are encouraged to participate in civic affairs.

7.2 PROJECT SPECIFIC PROFESSIONAL RESPONSIBILITY AREAS

Work Competence: This applies to our project because high-frequency analysis requires very precise equipment, so if we are meant to make a working DAQ, we must perform competently. We are performing medium because we haven't had a chance to show our competence, but we are making appropriate preparations.

Financial Responsibility: While we will avoid unnecessary expenses, the reality is that this device requires expensive components, so there are only so many cutbacks we can make without sacrificing quality. Our performance is N/A since we have yet to purchase components.

Communication Honesty: With such a complicated device, keeping open and detailed notes for both the client and ourselves is crucial. We are doing medium again since we have been documenting diligently, but so far, there needs to be more to document.

Health, Safety, Well-Being: All electrical devices are dangerous to some extent, so we will have to design ours to be contained and insulated so the user isn't shocked. We are performing N/A because we have done very little work on physical components.

Property Ownership: We will be using components given to us by the client, so keeping those components contained to the project is crucial. It would be incredibly inappropriate to take any designs that weren't created expressly by our team. Our performance is N/A since we have not yet used any components that weren't purchased from a third party.

Sustainability: We're still determining how to implement this effectively other than avoiding excessive power usage. We could also possibly take sustainability into consideration when making the final container. We are doing N/A again because we have done very little work with any physical components.

Social Responsibility: Our device will not make a large social impact, nor will it help general communities. Its effects and benefits will probably be contained to a niche group of electrical engineers. Our performance is N/A since I don't think this is very well applicable to our project.

7.3 MOST APPLICABLE PROFESSIONAL RESPONSIBILITY AREA

Honest communication is paramount to the success of our project, all of our tasks are dependent on the others, this means that we must be honest about what we have achieved and what we have struggled with. If we fail to communicate honestly and bluntly, we cannot expect to receive help, and or advice from our team members, and ultimately we would fail. Recently, one of our group members admitted that they felt a little lost at the moment, and that was just a good example of honest communication. I think we all feel unsure of what we are doing and I think we will improve as we go along. We have been very open with each other while speaking about project progress and we are grateful to have such discussions with each other. I think one of the impacts that our communication style has created is less stress within each group member, at least in regards to worrying about other members' contributions.

8 Closing Material

8.1 DISCUSSION

While we have no real results yet, we know very well what our goals and expectations are for the next semester. We have made a lot of hardware progress and have the infrastructure to complete the software portion. We expect a functioning DAQ equipped with a DAC and ADC that properly converts digital inputs into high-frequency waves and vice versa. We will also have an intuitive user interface for our client. Implementation and testing will begin within the first few months of the next semester.

8.2 CONCLUSION

So far, we have completed the hardware schematics and some limited testing of its functionality. We have also collected the necessary software tools to complete the FPGA's functionality as a millimeter wave DAQ. We've also gotten a reliable interface between our computers and the FPGA through our attached USB. In other words, we have all the ingredients ready to put together next semester.

We believe that we would have a significant amount of the project done now without the many assignments in the Senior design course. We hope to have more time and energy reserved for making actual progress rather than doing somewhat irrelevant documentation.

8.4 APPENDICES

References:

[1] C. Iovescu and S. Rao, "The fundamentals of millimeter wave radar sensors" Texas Instruments, Dallas, Texas Tech. Rep. SPYY005A, July 2020

Datasheets Used:

Programmer Guides (D2XX/D3XX drivers):

https://ftdichip.com/wp-content/uploads/2020/07/AN_379-D3xx-Programmers-Guide-1.pdf

[https://www.ftdichip.com/Support/Documents/ProgramGuides/D2XX_Programmer's_Guide\(FT_o00071\).pdf](https://www.ftdichip.com/Support/Documents/ProgramGuides/D2XX_Programmer's_Guide(FT_o00071).pdf)

Alchitry Schematics:

https://cdn.sparkfun.com/assets/2/5/3/6/o/Alchitry_Ft.pdf (Alchitry Ft (FTDI chip))

https://cdn.sparkfun.com/assets/b/6/2/f/b/alchitry_au_sch_update.pdf (FPGA PCB)

FTDI schematic (FTDI 600Q):

https://ftdichip.com/wp-content/uploads/2020/07/DS_FT600Q-FT601Q-IC-Datasheet.pdf

AD9767 DAC:

https://www.analog.com/media/en/technical-documentation/data-sheets/AD9763_9765_9767.pdf

ADC12DC105:

https://www.ti.com/lit/ds/symlink/adc12dc105.pdf?ts=1682308632947&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FADC12DC105

Work Examples:

Nathan Ayers:

```

#include <stdio.h>
#include <stdarg.h>
#include <stdlib.h>
#include <windows.h>
#include <windef.h>
#include <winnt.h>
#include <winbase.h>
#include <string.h>
#include <math.h>
#include <stdbool.h>
#include <stdint.h>
#include "C:\Users\nayer\CDM v2.12.36.4 WHQL Certified\ftd2xx.h"
#include <sys/time.h>

int main(){
    FT_STATUS ftStatus;
    FT_HANDLE ftHandle;
    FT_DEVICE_LIST_INFO_NODE *devInfo;
    DWORD numDevs;
    // create the device information list
    ftStatus = FT_CreateDeviceInfoList(&numDevs);

    if (ftStatus == FT_OK) {
        printf("Number of devices is %d\n",numDevs);
    }

    if (numDevs > 0) {
        // allocate storage for list based on numDevs
        devInfo =
(FT_DEVICE_LIST_INFO_NODE*)malloc(sizeof(FT_DEVICE_LIST_INFO_NODE)*numDevs
);
        // get the device information list
        ftStatus = FT_GetDeviceInfoList(devInfo,&numDevs);

        if (ftStatus == FT_OK) {
            for (int i = 0; i < numDevs; i++) {
                printf("Dev %d:\n",i);
                printf(" Flags=0x%x\n",devInfo[i].Flags);
                printf(" Type=0x%x\n",devInfo[i].Type);
                printf(" ID=0x%x\n",devInfo[i].ID);
                //printf(" LocId=0x%x\n",devInfo[i].LocId);
                printf(" SerialNumber=%s\n",devInfo[i].SerialNumber);
                printf(" Description=%s\n",devInfo[i].Description);
                printf(" ftHandle=0x%x\n",devInfo[i].ftHandle);
            }
        }
    }
}

```

```

    }
}
ftStatus = FT_Open(o, &ftHandle);
if (ftStatus == FT_OK) {
    // FT_Open OK, use ftHandle to access device
    printf("Yay, I work!\n");
}
else {
    // FT_Open failed
    printf("Ouch\n");
}
}
}

```

The code can be a little difficult to read, but the above code shows three of our D2XX/FTDI functions in use by a program. The first function, highlighted in green builds a device information list and then returns the number of devices connected. The second function, highlighted in yellow returns a device information list, essentially populating it given the number of devices. The third function, highlighted in blue simply opens the device and returns a handle to be used for subsequent accesses. All of these functions are honestly just for checking, helpful to an automated system, but still helpful in telling me that I am doing something right.

Code Output:

```

PS C:\Users\nayer\D2XX> gcc -o main anything.c -L"C:\Users\nayer\CDM v2.12.36.4 WHQL
Certified\i386" -lftd2xx
PS C:\Users\nayer\D2XX> ./main
Number of devices is 1
Dev o:
Flags=0x2
Type=0x8
ID=0x4036014
SerialNumber=FTYI9TEQ
Description=C232HM-EDHSL-o
ftHandle=0x0
Yay, I work!

```

So this code returned all of the output that was expected so it was a success!

Blink Code (Makes GPIO pins blink, technically a square wave with 1 Hz frequency):

```

do{
    printf("c = %d\n", c); // Just to check our count essentially
    if (val == 0xff)
    {
        val = 0;
    }
}

```

```

}
else
{
    val = 0xff;
}
byOutputBuffer[0] = 0x80;
    // configure data bits low-byte of MPSSE port
c++;
byOutputBuffer[1] = val; // actual data, essentially high or low
    // initial state config above

byOutputBuffer[2] = 0xff; //which pins are out/in
    // direction config above;

printf("byOutputBuffer[1] = %d, dwNumBytesToSend = %d\n",byOutputBuffer[1], 3);

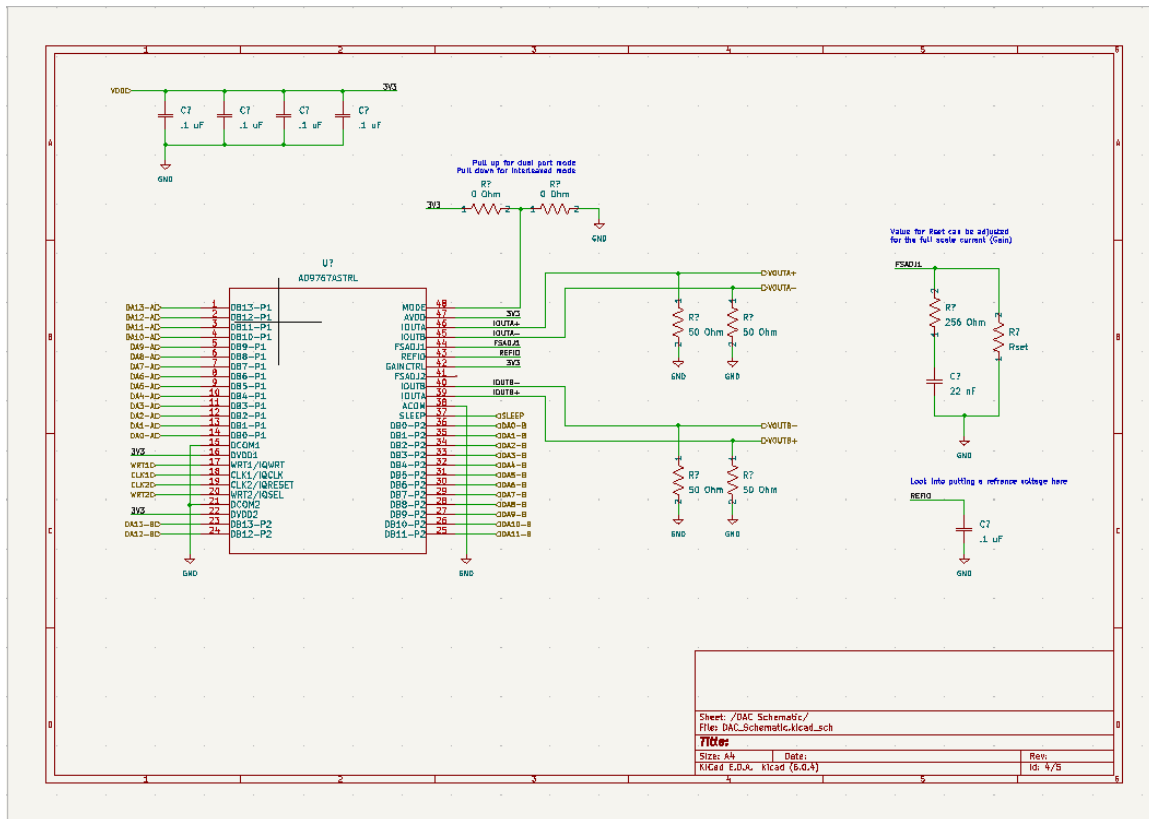
ftStatus = FT_Write(ftHandle, byOutputBuffer, 3, &dwNumBytesSent);
    // send off the high GPIO config commands
    dwNumBytesToSend = 0;
    Sleep(miliseecs);

}while(c<count*2);

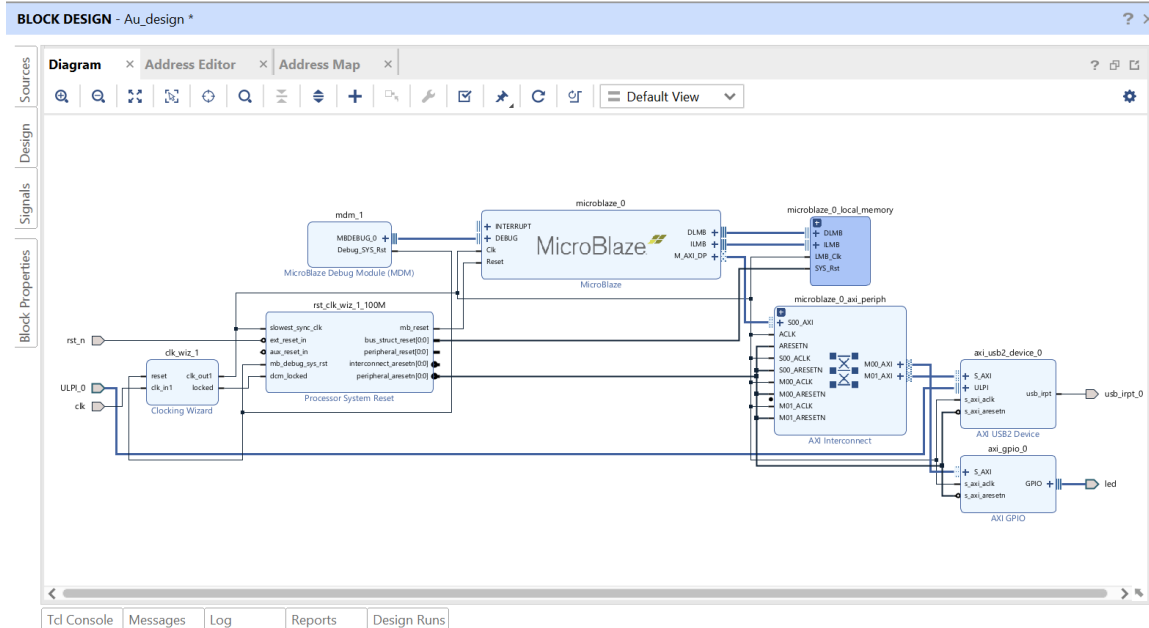
```

This is just a portion of the blink code but it is the only part that has to do with the blinking, I learned from various online resources that the pins can be controlled with a series of three hexadecimal numbers, each one byte. The first number determines which pins we are referring to, that doesn't apply to this cable I am using now as there are only 8 pins. The second number refers to data value of the output pins ie. the ones you are writing to. I just went back and forth between 0xFF and 0x00 to ensure high to low switching every second. The last number refers to the direction of the pins, with 1 being output and 0 being input. I found that this code works and set up an LED to the GPIO pins and it blinked every second for 10 seconds. It could be better and it will be better as I work on it more.

Matthew Caron:



This is the first draft of the schematic we will use for the DAC. All of the traces on the PCB should be matched to 50 Ohms.



The above picture is a sample of the design and layout of the FPGA we will use it includes a microblaze processor (shown in the middle of the photo) and a usb to ulpi device as well as a axi-gpio port that the microblaze processor uses to communicate with outside world.

Any additional information that would be helpful to the evaluation of your design document.

If you have any large graphs, tables, or similar data that does not directly pertain to the problem but helps support it, include it here. This would also be a good area to include hardware/software manuals used. May include CAD files, circuit schematics, layout etc.,. PCB testing issues etc.,. Software bugs etc.

8.4.1 Team Contract

Team Members:

- 1) Michael Levin
- 2) Matthew Caron
- 3) Rodrigo Romero
- 4) Nathan Ayers

Team Procedures

1. Day, time, and location (face-to-face or virtual) for regular team meetings:
Typical Meeting dates are every other Thursday at 3:00 PM with our advisor, additional meetings with just group members will likely occur more frequently as the project progresses.
2. Preferred method of communication updates, reminders, issues, and scheduling (e.g., e-mail, phone, app, face-to-face):
We communicate mostly through text messaging, and our meetings with Dr. Tayeeb are face-to-face. Our meeting schedule is shared with all group members through their outlook calendars.
3. Decision-making policy (e.g., consensus, majority vote): In most cases, the decision will be up to the group member that has expertise on the issue, if the rest of the group is concerned, then it will likely go to a majority vote policy.
4. Procedures for record keeping (i.e., who will keep meeting minutes, how will minutes be shared/archived): Every person will keep their own time record, and we will keep each other accountable of the recorded time.

Participation Expectations

1. Expected individual attendance, punctuality, and participation at all team meetings:
Everyone is expected to attend all the meetings at the agreed time. When a member does not attend a meeting he will be expected to ask questions about the meeting and get himself updated to keep the entire team in the same page.
2. Expected level of responsibility for fulfilling team assignments, timelines, and deadlines:
Every member of the team is expected to be responsible of his own actions and decisions regarding the assignments, timelines, and deadlines for the subsection of the project that each of us are leading. The expectations are that we will keep accountable each other

3. Expected level of communication with other team members: Every member is expected to keep communication with the rest of the team during the entire project. No ghosting is accepted by any means.
4. Expected level of commitment to team decisions and tasks: Every team member is expected to make the best decisions for the sake of the project, and work for the best possible quality.

Leadership

1. Leadership roles for each team member (e.g., team organization, client interaction, individual component design, testing, etc.):
Team Organization: Michael Levin
Client interaction: Matthew Caron
Design & Testing: Matthew(PCB), Rodrigo and Michael(FPGA), Nathan(PC Software)
2. Strategies for supporting and guiding the work of all team members: To keep accountability during the project we will interact with each other in couples. Matt Caron will keep Rodrigo Romero accountable and vice versa as well as Michael Levin will keep Nathan Ayers accountable and vice versa.
3. Strategies for recognizing the contributions of all team members: In terms of time contribution, we have a system that keeps track of that. More important contributions include milestone completion and those will be experienced by the whole group to ensure that the group member that completed a task is recognized.

Collaboration and Inclusion

1. Describe the skills, expertise, and unique perspectives each team member brings to the team.
 - a. Michael Levin: Experience in Matlab and Matlab app designer, using high frequency devices, signal processing and analysis, using shop tools and 3D printers.
 - b. Nathan Ayers: Programming experience in C, C++, Java, Python, EE focus on VLSI with a preference for using Verilog over VHDL. I have broad experience with tools, which should be helpful if we need to design a box.
 - c. Rodrigo Romero: Workshop machining, solidworks, Fusion 360, writing skills, CST studio, verilog, MATLAB, Simulink.
 - d. Matthew Caron: Programming experience (C++, C, Python, MATLAB), circuit design, Kicad, Altium, 3D printing.
2. Strategies for encouraging and support contributions and ideas from all team members:
 - a. As members finish their individual parts, they will partner with the member in charge of the next component to be implemented. This allows for more and more voices to be heard as the project progresses to ensure all of the components are function together.
3. Procedures for identifying and resolving collaboration or inclusion issues (e.g., how will a team member inform the team that the team environment is obstructing their opportunity or ability to contribute?)
 - a. If a team member has issues that they feel are caused by the group dynamic, they should discuss the issues as soon as possible with other group members. We all prefer a direct style of communication so we would prefer honesty and being straightforward.

Goal-Setting, Planning, and Execution

1. Team goals for this semester: Have a well structured plan for the project's execution during the Fall 2023 semester, the plan must include a detailed timeline. Another goal for the Spring 2023 semester is that every member of the team will be able to explain the project in a presentation format, and what we are going to execute it during the Fall semester.
2. Strategies for planning and assigning individual and team work:
Our work has been assigned based on what we feel are our strongest attributes within the group, additional tasks will be assigned based on current work load at the time, if they are trivial tasks,
3. Strategies for keeping on task:
We are accountable for each other, if that doesn't motivate us to stay on task, we will be pushed by our group members to complete our work in a timely manner.

Consequences for Not Adhering to Team Contract

1. How will you handle infractions of any of the obligations of this team contract? If any of the team members happen to not attend a meeting (even if he make an announcement in advance) he will need to bring pizza and pop for the next meeting.
2. What will your team do if the infractions continue? If the infraction continues the team member will need to arrange an extraordinary meeting during a weekend and he will make a 30 minutes presentation for the rest of the team explaining how he caught up based on conversations with the rest of the team, the presentation must include a brief refresh of the overall project. He will bring donuts and coffee (or orange juice) for that extraordinary meeting.

- a) I participated in formulating the standards, roles, and procedures as stated in this contract.
- b) I understand that I am obligated to abide by these terms and conditions.
- c) I understand that if I do not abide by these terms and conditions, I will suffer the consequences as stated in this contract.

- 1) _____ Rodrigo Romero _____ DATE __02/16/2023_____
- 2) _____ Nathan Ayers _____ DATE __02/16/2023_____
- 3) _____ Matthew Caron _____ DATE __02/18/2023_____
- 4) _____ Michael Levin _____ DATE __02/18/2023_____