IOWA STATE UNIVERSITY
College of Engineering

PIRM Presentation 2

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Problem Statement

Who? Our client, Dr. Al Qaseer and the CNDE conduct research into evaluating a system or structure without affecting its future usability and functionality.

What? The CNDE needs a new mm-Wave radar to be built for student research experiments.

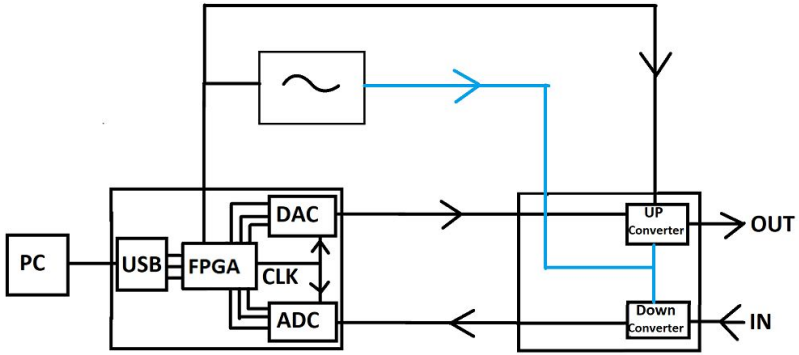
Why? Millimeter-Wave technology has been used to penetrate dielectric materials and has a high sensitivity to small material flaws. Research benefits safety and can help companies increase sustainability.

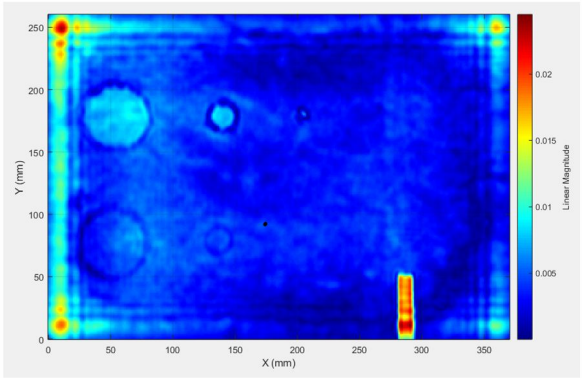
When? Students are already experimenting with samples that have errors designed to test the imaging. The applications will continue to grow and the technology will impact everyone.

Project Topic

Millimeter Wave Data Acquisition Device:

- Make scans of materials beyond its surface nondestructively
  - Finds defects within the sample
  - Can determine various properties of the sample
- Generates up to 40 GHz wave and collects signal reflection

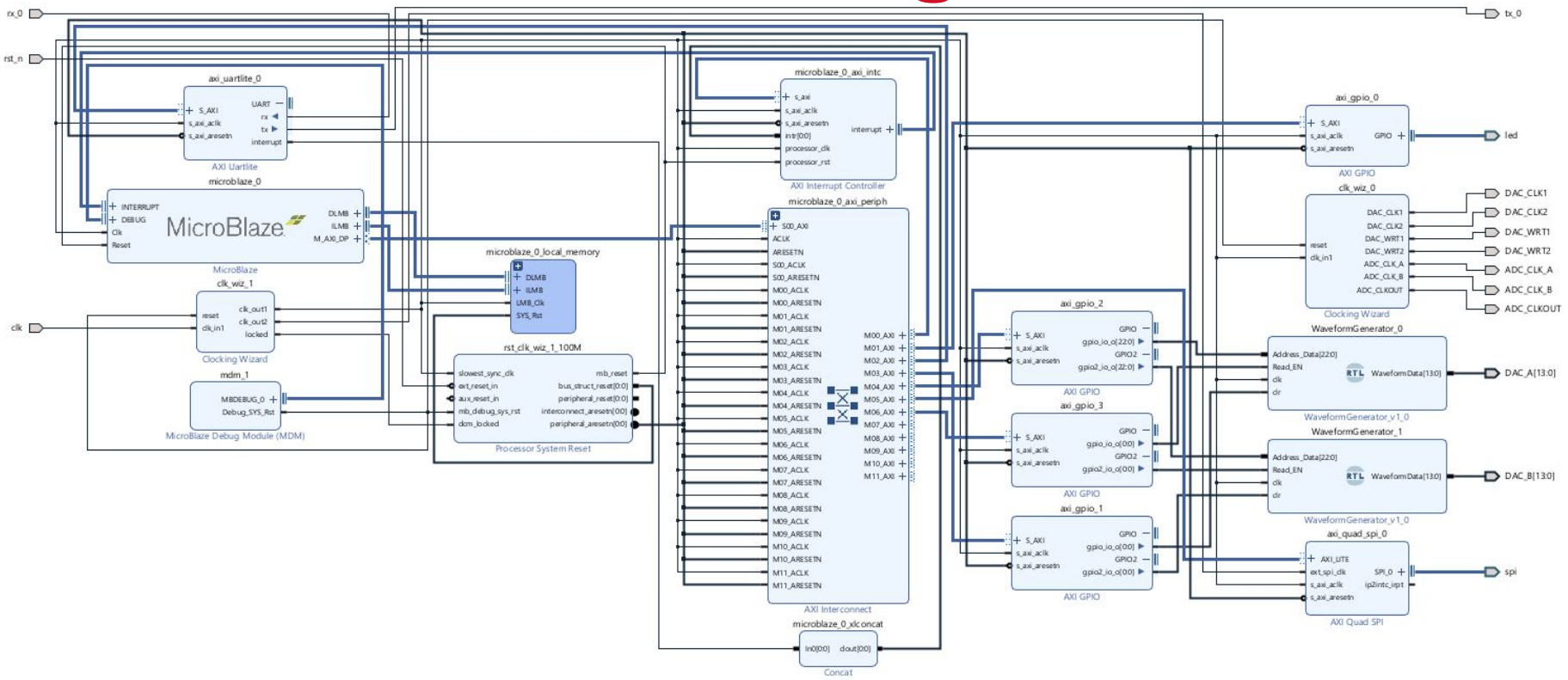




Where We're At

- PCB/SPI
  - PCB is completed and in the process of being assembled and tested. SPI is currently being implemented in the FPGA design to program the necessary up and down converter registers
- USB Interface
  - Since our design uses the FT600q we need to update our library code for the PC to interface with the FPGA as well as creating the hardware interface so the FPGA can interact with the FT600q
- DAC writing
  - Arbitrary function generator is completed so we can continuously clock out an arbitrary periodic signal to the DAC at each clock cycle
- ADC reading
  - Currently working on the FPGA hardware for reading and processing ADC data

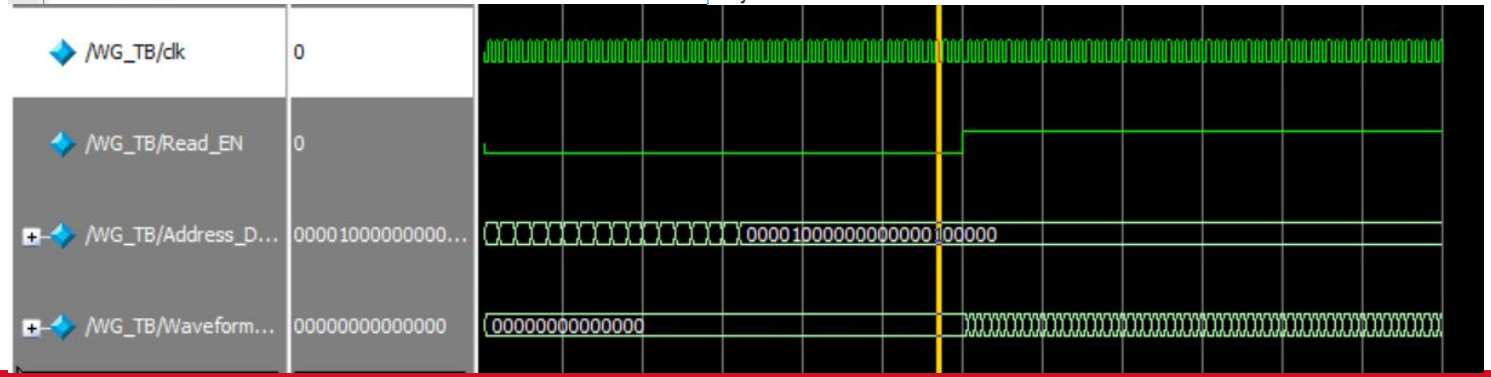
FPGA hardware design



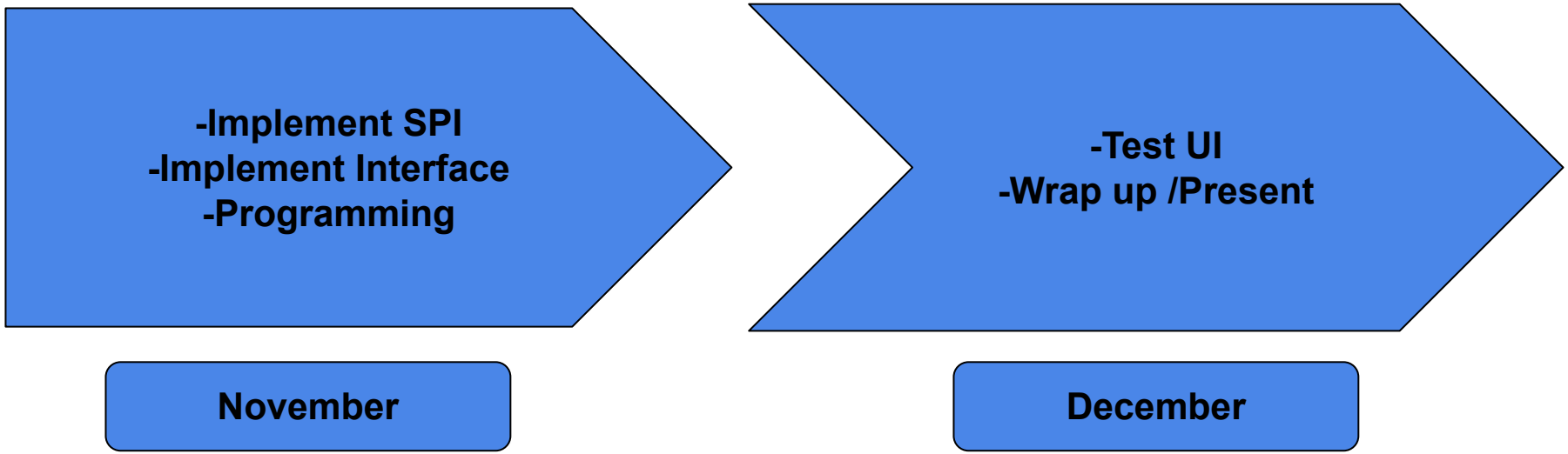
Programmable Function Generator

```
module WaveformGenerator(
        input [22:0] Address_Data,
        input Read_EN,
        input clk,
        output reg [13:0] WaveformData = 14'h000
    );
        reg [8:0] curr_address = 9'h000;
        reg [8:0] iter = 9'h000;
        reg [8:0] max_address = 9'h000;
        reg [13:0] storageData [0:512];

        always @ (posedge clk) begin
                if (Read_EN) begin
                        WaveformData <= storageData[iter];
                end
        end

        always @ (posedge clk) begin
                if (~Read_EN) begin
                        curr_address = Address_Data >> 14;
                        storageData[curr_address] = Address_Data & 14'h3FFF;
                end
        end

        always @ (negedge clk) begin
                if (Read_EN) begin
                        iter = (iter < max_address) ? (iter + 1'b1): 9'h000;
                end
        end

        always @ (negedge clk) begin
                if (~Read_EN) begin
                        max_address = (curr_address > max_address) ? curr_address: max_address;
                end
```

```
// writes waveforms into the function generator
void writeDAC_RAM(u16 *DAC_Function, u8 channel, u16 sizeofFunct)
{
    //XGpio_DiscreteWrite(&Clear_Waveform, channel, 0x1);
    //XGpio_DiscreteWrite(&Clear_Waveform, channel, 0x0);
    u32 address;
    u32 address_data;
    XGpio_DiscreteWrite(&EN_READ, channel, 0x0); //Enable Write to RAM

    // Write the data in DAC waveforms to the RAM
    u16 i;
    u32 j;
    for (i = 0; i < sizeofFunct; i++)
    {
        address = i << 14;
        address_data = address | *(DAC_Function + i);
        XGpio_DiscreteWrite(&Data_Address_DAC, channel, address_data);
        XGpio_DiscreteWrite(&LEDS, 1, 0xFF & address_data >> 14);
    }
    XGpio_DiscreteWrite(&EN_READ, channel, 0x1); //Disable Write to RAM
    XGpio_DiscreteWrite(&LEDS, 1, 0x01);
}
```



Project Milestones Ahead



Technical Challenges

- Availability of information
  - Online resources for the FTDI drivers(USB comm), Vivado(FPGA programming) and Alchitry(FPGA board) are scarce.
  - Reaching out to people with similar project experience.
- Component Constraints
  - Difficult to find components that will function properly with our assigned FPGA development board.
  - Solved by investing more time into part sourcing.
- Work methodology
  - The implementation is similar to a ladder.
  - We can avoid issues by communicating about interface needs.

New Technical Challenges

- Lack of continuity between FTDI libraries
  - USB programming originally done with D2XX library, but final design will be in FT60x.
  - There is very little compatibility between the two libraries, and function differs greatly.
- More documentation issues
  - FTDI FT600 has very little documentation available, and Alchitry doesn't supply information.

Thank you for listening to our presentation!

Questions?