***EE/CprE/SE 491 WEEKLY REPORT***

***Start Date – End Date***

***Group number: 20***

***Project title: mm Wave Imaging radar***

***Client &/Advisor: Mohammed Tayeb Al Qaseer***

***Team Members/Role: Nathan Ayers: Interface Lead, Rodrigo Romero: Lead FPGA Programming Engineer, Michael Levin: Lead DSP Engineer, Matthew Caron: Lead Hardware Designer.***

- **Weekly Summary**

This week was spent getting a hold of each of our assignments. There are several details that were not clear to many of us on the team so we talked to each other and our client to get a clear picture of what was being asked of us and how we are to accomplish it.

- **Past week accomplishments** *(Please describe/summarize as to what was done, by whom, when and, collectively as a group. This should be about a paragraph or two in length. Bulleted points are acceptable as well. Please keep only your technical details related to your project. Figures, schematics, flow diagrams, pseudocode, and project related results are acceptable, but please ensure that they are legible (clear enough to read) and to provide an explanation. If researching a topic, please add a few details about what was learned and how it is relevant to the project. If two or more people worked on a single task, be sure to distinguish how each member contributed to the task. Specific details relating to the assistance provided to other members may be included here.* ***Do not include classwork, such as individual reflection assignments, and group meetings as part of your duties.)***
    - Nathan Ayers: Was able to research the FTDI chip that I will use for the PC interface to the FPGA, I installed a driver that will allow me to communicate with said chip and I began to set up my programming environment.
    - Rodrigo Romero: Did not contribute to the project. I was struggling with extracurricular activities.
    - Michael Levin: I started doing simple calculations with vivado.
    - Matthew Caron: Worked on organization with Gitlab, some testing with the FPGA (what voltage input ranges can be used), and finished up the schematic for interfacing with the DAC.
- **Pending issues** *(If applicable: Were there any unexpected complications? Please elaborate.)*
    - Nathan Ayers: Limited access to the FPGA will limit my progress, as I will not have many opportunities to test my work, but I'm not very worried about that yet.

- Rodrigo Romero: Continue to work in the learning environment of FPGA using Alchitry lab.
- Michael Levin: I haven’t done any complicated calculations with vivado yet.
- Matthew Caron: Get the ETG to help import the Alchitry Au+ drivers to Vivado since the ISU firewall was preventing a bit of work this weekend.

- **Individual contributions** *(Creating this section is optional, but it is **Required to include the "Hours Worked for the Week" and their "Total Cumulative Hours" for the project for each member somewhere relevant in your report. Your individual weekly hours should be at a minimum of 6-8 hours for this course. So please manage your time well. Also, ensure that individual contributions support your claim to the weekly hours. Be honest with the reports.**)*

| NAME | Individual Contributions *(Quick list of contributions. This should be short.)* | Hours this week | HOURS cumulative |
|---|---|---|---|
| Michael Levin | I set up the report and contributed to the group assignments. I also participated in the meeting with our client. | 3 | 12 |
| Nathan Ayers | Was able to research the FTDI chip that I will use for the PC interface to the FPGA, I installed a driver that will allow me to communicate with said chip and I began to set up my programming environment. I completed the lightning talk presentation and Speaker notes that accompany it, and worked on the separate Standards document. | 3 | 12 |
| Rodrigo Romero | No contributions this week. | 0 | 10 |
| Matthew Caron | Worked on organization with Gitlab, some testing with the FPGA (what voltage input ranges can be used), and finished up the schematic for interfacing with the DAC. | 4 | 13 |

- **Comments and extended discussion** *(Optional)*

  *Feel free to discuss non-technical issues related to your project.*

- **Plans for the upcoming week** *(Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.)*
  - Nathan Ayers: interfacing with the FTDI chip, hopefully I can successfully turn pins on and observe with an oscilloscope.
  - Rodrigo Romero: Get updated about the team meeting from last week, and continue learning FPGA in Alchitry lab environment.
  - Michael Levin: I plan on trying to do laplace transforms in vivado.
  - Matthew Caron: find an ADC that will work and continue testing on the FPGA

- **Summary of weekly advisor meeting**

  We met with Dr. Tayeeb this week and he clarified many of our questions that we came with. If we learned any new information, we will include below individually.

  - Nathan learned: The research I had been doing was not specific enough and therefore not very helpful to me, I needed to learn how to communicate with a specific chip, requiring a

specific driver installation. I'm definitely out of my comfort zone but I am glad to be pushed in the right direction. I feel much more confident than this time last week.

**Grading criteria**

Each weekly report is worth 10 points. Scores will be awarded as follows:

- **8 – 10**: Progress for your project seems to be suitable. Documentation and hours reported by team members are adequate.
- **6 – 8**: There is scope of improvement both in your report and your project progress. Can consult with instructor/TA after class for further inputs.
- **< 6**: Please talk to instructors/TA after class hours about any difficulties that you/your team is facing.

Each weekly report should be unique in that they have a unique set of supporting details for your contributions. So please do not just copy your reports from the previous week. In addition, please avoid any personal pronouns (he, she, I, you). Try to keep your reports as neat as possible.