EE/CprE/SE 491 WEEKLY REPORT

3/6/23 – 3/12/23

Group number: 20

Project title: mm Wave Imaging radar

Client &/Advisor: Mohammed Tayeb Al Qaseer

Team Members/Role: Nathan Ayers: Interface Lead, Rodrigo Romero: Lead FPGA Programming Engineer, Michael Levin: Lead DSP Engineer, Matthew Caron: Lead Hardware Designer.

(All the above information should be there in each weekly report. The format/color scheme etc need not be the same. However, please remove everything that is in a bracket from your final submission. These are just part of the template and need not be a part of the report.)

- **Weekly Summary**
  This week we had a group meeting with just the project members, everybody attended, we had more discussion about the FPGA, we talked about Rodrigo's part in the project and we hope that he gained some insight into the FPGA. The group agreed that Matt should take the FPGA for experimentation over Spring Break.

- **Past week accomplishments**
  - Nathan Ayers: Besides the weekly meeting, I completed no project specific tasks worth noting.
  - Matthew Caron: worked on the pcb schematic as well as trying to get the FPGA outputting a 1.8V single ended signal
- **Pending issues** *(If applicable: Were there any unexpected complications? Please elaborate.)*
  - Nathan Ayers: Access to FPGA is a continuing issue that we all have, but the priority is Matt's work at the moment.
  - Michael Levin: I wasn't able to do much work with vivado because my internet was down during the time that I needed to do research on how to program in it.
  - Matthew Caron: not too many pending issues besides the little ones that always arise with any design.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Michael Levin	I contributed in the weekly meeting and did some more simple algebra in vivado but it wasn't significant.	1	13
Nathan Ayers	Besides the weekly meeting, I completed no project specific tasks worth noting.	1	13
Matthew Caron	worked on the pcb schematic as well as trying to get the FPGA outputting a 1.8V single ended signal	2	15

- **Plans for the upcoming week**
  - Nathan Ayers: I have no plans for the next week, I have Spring Break plans that take me away from the project outside of emergencies.
  - Michael Levin: I plan on using my break to try more complicated calculations in vivado.
  - Matthew Caron: I plan on working the schematic more as well as a little FPGA layout

Grading criteria

Each weekly report is worth 10 points. Scores will be awarded as follows:

- **8 – 10**: Progress for your project seems to be suitable. Documentation and hours reported by team members are adequate.
- **6 – 8**: There is scope of improvement both in your report and your project progress. Can consult with instructor/TA after class for further inputs.
- **< 6**: Please talk to instructors/TA after class hours about any difficulties that you/your team is facing.

Each weekly report should be unique in that they have a unique set of supporting details for your contributions. So please do not just copy your reports from the previous week. In addition, please avoid any personal pronouns (he, she, I, you). Try to keep your reports as neat as possible.