EE/CprE/SE 492 BIWEEKLY REPORT 1

08/21/2023 – 09/15/2023

Group number: 20

Project title: mmWave device for non-destructive evaluation

Client &/Advisor: Center for Non-Destructive Evaluation. Mohammad Tayeb Al Qaseer, Ph.D.

Team Members/Role:

Matthew Caron - Hardware lead

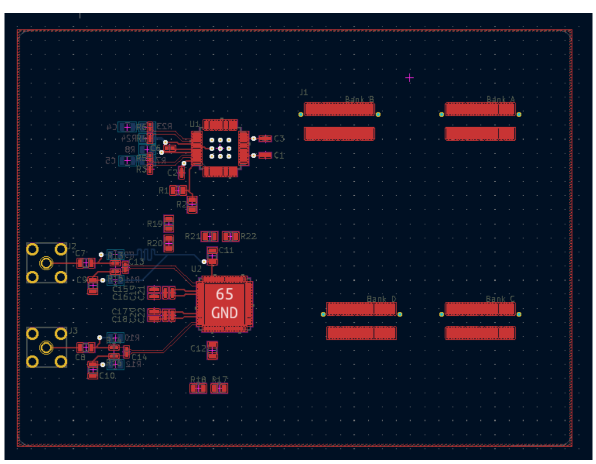
Rodrigo Romero - Lead FPGA Engineer

Michael Levin - Lead DSP Engineer

- **Weekly Summary**
  - The start of this semester was spent getting our bearings and making a plan. We made progress on the individual pieces of the projects and updating each other on what still needs to get done. We then used that information to plan an optimal and worse case schedule for the completion of our project and presentations throughout the semester.

- **Past week accomplishments**
  - Matthew Caron: Completed design of the schematic for the PCB we will use for data acquisition of the IQ signals. Moved onto layout of the PCB and got the critical circuitry of the ADC and DAC layed out. Now currently working on connecting outputs/inputs of the circuitry to the FPGA data lines.

    PCB Layout:



- Nathan Ayers: Developed a PWM program to utilize the GPIO ports on a FTDI chip, I then attached those to a breadboard with LEDs to show that the Pulses were generating properly. This allowed me to recognize which bit represented each data port on my FTDI cable. I am still trying to figure out how to read those pins as I am struggling to match the output written to a pin to the input.
- Rodrigo Romero: Reached out to the client/academic advisor to talk about my specific duties in the project. I received the technical data sheets of the downconverter and upconverter we will use for the project. I am on charge of establish communication between the FPGA and the mentioned converters.
- Michael Levin: I created the Microblaze block in vivado and surrounding class infrastructure around it as well as some debugging. I also made the tentative schedule for the project for the rest of the semester and created the presentation and report for the next couple weeks.

o **<u>Pending issues</u>**

- Matthew Caron: work on software to take in the data from the ADCs and send data to the DACs
- Nathan Ayers: I have no issues in terms of SW or HW.
- Rodrigo Romero: I have to figure out what register of the converters I have to establish communication with in order to connect them to the FPGA.
- Michael Levin: There are some errors that come from the lack of outputs in the code.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this period**	**HOURS cumulative**
Matthew Caron	PCB: schematic design, and layout	6	30
Nathan Ayers	FTDI programming I/O and GUI	9	54
Rodrigo Romero	FPGA progress in understanding downconverter and upconverter.	7	31
Michael Levin	Microblaze progress, made semester project schedule, and made the templates for our reports and presentations.	10	32

- **Comments and extended discussion** *(Optional)*
  Established a clear schedule and deadlines to hold ourselves accountable for the work we agreed to do

- **Plans for the upcoming week** *(Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.)*
  - Matthew Caron: Finish up layout of the PCB so we can work on team board review this week so we can work on ordering the board before the end of the month.
  - Nathan Ayers: My plan is to create actual binary strings through the FTDI chip, and then to be able to read the exact output as an input. What I need is to find continuity between what I send out through the FTDI and what I receive back.
  - Rodrigo Romero: The establishment of communication between the FPGA and the converters using the data sheets will be achieved.
  - Michael Levin: I'm going to make a new vivado project to repeat my steps and see if I can find the output errors that way. I'm also going to work with my group on our upcoming presentation.